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EXAMINER	
YIGDALL, MICHAEL J	
ART UNIT	**PAPER NUMBER**
2192	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/780,264	WOLCZKO ET AL.	
	Examiner	Art Unit	
	Michael J. Yigdall	2192	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *04 May 2009*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-18 and 20-23* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-18 and 20-23* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. This Office action is responsive to Applicant's reply filed on May 4, 2009. Claims 1-18 and 20-23 are now pending.

Response to Arguments

2. Applicant's arguments have been fully considered but they are not persuasive.

Applicant contends that there is "simply no teaching or suggestion in Kalafatis of reporting anything to any particular thread" such as recited in claim 1. Applicant states that instead, "Kalafatis teaches that external software accesses and samples the contents of event counters via a program instruction" (remarks, page 6).

However, the examiner submits that accessing and sampling the contents of the event counters does, in fact, represent "reporting" the contents of the event counters. For example, Kalafatis clearly describes, "The contents of the event counters can be accessed and sampled via a program instruction thus providing information concerning processor performance" (column 2, lines 52-54; emphasis added). Thus, Kalafatis teaches "reporting the sampling information" such as recited in the claim.

In response to Applicant's further contention that Kalafatis "teaches the opposite of claim 1" (remarks, page 6), the examiner submits that reporting the information from the threads to the event counters actually represents "storing sampling information" such as recited in the claim. In other words, aside from "reporting the sampling information" from the event counters, Kalafatis also teaches "storing [the] sampling information" in the event counters.

Applicant contends that there is "simply no teaching or suggestion in Kalafatis of when any reporting occurs." Applicant states that Kalafatis "merely qualifies events for storage to event counters … and does not teach conditionally storing information based upon whether the information includes an event of interest" such as recited in claim 1 (remarks, page 6).

First, however, Kalafatis clearly teaches that the information is reported when a RDMSR instruction is executed (see, for example, column 6, lines 1-14 and 29-40). Second, Kalafatis clearly teaches an event selection control register for selecting events of interest (see, for example, column 4, lines 19-30). Thus, Kalafatis teaches "conditionally storing information" based on whether the information includes an event of interest (see FIG. 1).

Applicant further contends that Chrysos "does not teach conditionally reporting sampling information for a particular thread" and "simply reports sampling information unconditionally" (remarks, page 6).

However, as set forth in the Office action, Chrysos teaches filtering the sampling information for a particular thread (see, for example, column 12, lines 1-4). Moreover, Chrysos teaches reporting a subset of the sampling information based on a function (see, for example, function 755 in FIG. 7B and column 17, lines 34-61). Thus, Chrysos teaches "conditionally reporting sampling information" based on the function.

In summary, Applicant is respectfully reminded that the test for obviousness is not that the claimed invention must be expressly suggested in any one or all of the references. Rather, the test is what the combined teachings of the references would have suggested to those of ordinary skill in the art. See *In re Keller*, 642 F.2d 413, 208 USPQ 871 (CCPA 1981). For at

least the above reasons, the examiner submits that the combined teachings of Chrysos and Kalafatis would have suggested the claimed invention to those of ordinary skill in the art.

Claim Rejections under 35 U.S.C. § 103

3. The following is a quotation of 35 U.S.C. § 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 1-18 and 20-23 are rejected under 35 U.S.C. § 103(a) as being unpatentable over U.S. Patent No. 6,000,044 to Chrysos et al. (already of record, "Chrysos") in view of U.S. Patent No. 7,448,025 to Kalafatis et al. (already of record, "Kalafatis").

With respect to claim 1 (previously presented), Chrysos teaches a method of sampling instructions executing in a multi-threaded processor (see, for example, the abstract) comprising:

selecting an instruction for sampling (see, for example, column 10, lines 19-25, which shows selecting an instruction for sampling);

storing sampling information relating to the instruction (see, for example, column 11, lines 31-38, which shows storing such sampling information);

determining whether the sampling information includes an event of interest to a particular thread within which the instruction is executing (see, for example, column 15, lines 32-42, which shows filtering the sampling information for events of interest, and column 12, lines 1-4, which further shows filtering the sampling information based on the thread of execution).

Chrysos further teaches reporting the sampling information when the sampling information includes an event of interest (see, for example, FIG. 7B and column 17, lines 34-61), but does not explicitly describe:

reporting the sampling information to the particular thread when the sampling information includes an event of interest.

Nonetheless, one of ordinary skill in the art could, with predictable results, implement the teachings of Chrysos such that the sampling information is reported to the particular thread when the sampling information includes an event of interest to the particular thread.

For example, in an analogous art, Kalafatis teaches qualifying events of interest in a multi-threaded processor based on the particular thread that executes the instructions (see, for example, column 2, lines 39-55). Kalafatis describes that such qualification provides versatility in reporting the event information (see, for example, column 6, lines 41-58).

Therefore, in view of Kalafatis, it would have been obvious to those of ordinary skill in the art at the time the invention was made to implement the teachings of Chrysos so as to report the sampling information to the particular thread when the sampling information includes an event of interest.

With respect to claim 2 (previously presented), the rejection of claim 1 is incorporated, and Chrysos in view of Kalafatis further teaches or suggests providing a register with a bit vector representing a plurality of events of interest; and

wherein the determining whether the sampling information includes the event of interest further includes comparing the sampling information relating to the instruction to the bit vector (see, for example, column 16, lines 52-55).

With respect to claim 3 (previously presented), the rejection of claim 2 is incorporated, and Chrysos in view of Kalafatis further teaches or suggests that the comparing is via at least one of a mask operation or a more expressive operation (see, for example, column 16, lines 52-55).

With respect to claim 4 (original), the rejection of claim 1 is incorporated, and Chrysos in view of Kalafatis further teaches or suggests that the selecting the instruction is without regard to a thread to which the instruction is bound (see, for example, column 6, lines 48-49).

With respect to claim 5 (original), the rejection of claim 1 is incorporated, and Chrysos in view of Kalafatis further teaches or suggests identifying a thread to which the instruction is bound when the instruction is selected (see, for example, column 14, lines 53-64).

With respect to claim 6 (original), the rejection of claim 1 is incorporated, and Chrysos in view of Kalafatis further teaches or suggests providing filtering criteria on a per-thread basis (see, for example, column 15, lines 21-43).

With respect to claim 7 (original), the rejection of claim 1 is incorporated, and Chrysos in view of Kalafatis further teaches or suggests providing a single set of filtering criteria; and, scheduling sampling among a plurality of threads via software (see, for example, column 15, lines 21-43).

With respect to claim 8 (currently amended), Chrysos teaches a method of sampling instructions executing in a multi-threaded processor (see, for example, the abstract) comprising:

setting a candidate counter to a number (see, for example, column 14, lines 40-52, which shows setting a counter to a value);

selecting an instruction for sampling (see, for example, column 10, lines 19-25, which shows selecting an instruction for sampling);

storing information relating to the instruction (see, for example, column 11, lines 31-38, which shows storing such information);

determining whether all events for the instruction have occurred (see, for example, column 15, lines 43-49, which shows determining that all events for the instruction are complete).

Chrysos further teaches decrementing the counter (see, for example, column 14, line 64 to column 15, line 4) and filtering the information based on the thread of execution (see, for example, column 12, lines 1-4), but does not explicitly describe:

decrementing the candidate counter when all events for the instruction have occurred and when the instruction corresponds to a desired sampled thread.

Nonetheless, one of ordinary skill in the art could, with predictable results, implement the teachings of Chrysos such that the candidate counter is decremented when all events for the instruction have occurred and when the instruction corresponds to a desired sampled thread.

For example, in an analogous art, Kalafatis teaches qualifying events of interest in a multi-threaded processor based on the particular thread that executes the instructions (see, for example, column 2, lines 39-55). Kalafatis describes that such qualification provides versatility in reporting the event information (see, for example, column 6, lines 41-58).

Therefore, in view of Kalafatis, it would have been obvious to those of ordinary skill in the art at the time the invention was made to implement the teachings of Chrysos so as to decrement the candidate counter when all events for the instruction have occurred and when the instruction corresponds to a desired sampled thread.

Chrysos in view of Kalafatis further teaches or suggests:

determining whether the candidate counter equals zero (see, for example, column 14, line 64 to column 15, line 4, which shows determining that the counter underflows or overflows); and

reporting the instruction to a particular thread when the candidate counter equals zero (see, for example, FIG. 7B and column 17, lines 34-61, which shows reporting the information).

With respect to claim 9 (original), the rejection of claim 8 is incorporated, and Chrysos in view of Kalafatis further teaches or suggests that the information relating to the instruction represents an instruction history (see for example column 6, lines 48-49), and the instruction history includes information relating to at least one of an events value, a program counter value, a branch target address value, an effective memory address value, a latency value, a number in issue bundle value, a number in retire bundle value, a privilege value, a branch history value and a number in fetch bundle value (see, for example, column 6, lines 48-49).

With respect to claim 10 (original), the rejection of claim 8 is incorporated, and Chrysos in view of Kalafatis further teaches or suggests that the selecting the instruction is without regard to a thread to which the instruction is bound (see, for example, column 14, lines 53-64).

With respect to claim 11 (original), the rejection of claim 8 is incorporated, and Chrysos in view of Kalafatis further teaches or suggests identifying a thread to which the instruction is bound when the instruction is selected (see, for example, column 14, lines 53-64).

With respect to claim 12 (original), the rejection of claim 8 is incorporated, and Chrysos in view of Kalafatis further teaches or suggests providing filtering criteria on a per-thread basis (see, for example, column 15, lines 21-34).

With respect to claim 13 (original), the rejection of claim 8 is incorporated, and Chrysos in view of Kalafatis further teaches or suggests providing a single set of filtering criteria; and, scheduling sampling among a plurality of threads via software (see, for example, column 15, lines 21-34).

With respect to claim 14 (currently amended), Chrysos teaches a method of sampling instructions executing in a multi-threaded processor comprising:

setting a candidate counter to a number (see, for example, column 14, lines 40-52, which shows setting a counter to a value);

selecting an instruction for sampling (see, for example, column 10, lines 19-25, which shows selecting an instruction for sampling);

storing information relating to the instruction(see, for example, column 11, lines 31-38, which shows storing such information);

determining whether all events for the instruction have occurred (see, for example, column 15, lines 43-49, which shows determining that all events for the instruction are complete).

Chrysos further teaches filtering the information for events of interest (see, for example, column 15, lines 32-42) and filtering the information based on the thread of execution (see, for example, column 12, lines 1-4), but does not explicitly describe:

determining whether the instruction includes events of interest, the events of interest including whether the instruction corresponds to a desired sampled thread.

Nonetheless, one of ordinary skill in the art could, with predictable results, implement the teachings of Chrysos so as to determine whether the instruction includes events of interest, the events of interest including whether the instruction corresponds to a desired sampled thread.

For example, in an analogous art, Kalafatis teaches qualifying events of interest in a multi-threaded processor based on the particular thread that executes the instructions (see, for example, column 2, lines 39-55). Kalafatis describes that such qualification provides versatility in reporting the event information (see, for example, column 6, lines 41-58).

Therefore, in view of Kalafatis, it would have been obvious to those of ordinary skill in the art at the time the invention was made to implement the teachings of Chrysos so as to determine whether the instruction includes events of interest, the events of interest including whether the instruction corresponds to a desired sampled thread.

Chrysos in view of Kalafatis further teaches or suggests:

decrementing the candidate counter when all events for the instruction have occurred and when the instruction includes events of interest (see, for example, column 14, line 64 to column 15, line 4, which shows decrementing the counter);

determining whether the candidate counter equals zero (see, for example, column 14, line 64 to column 15, line 4, which shows determining that the counter underflows or overflows); and

reporting the instruction to a particular thread when the candidate counter equals zero (see, for example, FIG. 7B and column 17, lines 34-61, which shows reporting the information).

With respect to claim 15 (original), the rejection of claim 14 is incorporated, and Chrysos in view of Kalafatis further teaches or suggests providing a register with a bit vector representing events of interest; and

wherein the determining whether the instruction includes events of interest further includes comparing the information relating to the instruction to the bit vector (see, for example, column 16, lines 52-55).

With respect to claim 16 (original), the rejection of claim 14 is incorporated, and Chrysos in view of Kalafatis further teaches or suggests that the information relating to the instruction represents an instruction history, and the instruction history includes information relating to at least one of an event value, a program counter value, a branch target address value, an effective memory address value, a latency value, a number in issue bundle value, a number in retire bundle value, a privileged value, a branch history value and a number in fetch bundle value (see, for example, column 6, lines 48-49).

With respect to claim 17 (original), the rejection of claim 14 is incorporated, and Chrysos in view of Kalafatis further teaches or suggests that the selecting an instruction for sampling is based upon sample selection criteria; and

the sample selection criteria include information relating to a desired sampled thread (see, for example, column 15, lines 30-35).

With respect to claim 18 (currently amended), Chrysos teaches a multi-threaded processor (see, for example, FIG. 1) comprising:

a sampling logic configured to determine whether an instruction executed in the processor corresponds to a desired sampled thread (see, for example, column 10, lines 19-25, which shows determining that an instruction is selected for sampling);

a sampling register logic coupled to the sampling logic (see, for example, FIG. 2B);

an instruction history register logic coupled to the sampling register logic, the instruction history register logic storing information relating to the instruction (see, for example, column 11, lines 31-38, which shows storing such information);

a sample filtering and counting logic coupled to the sampling logic (see, for example, column 15, lines 32-42, which shows filtering, and column 14, line 64 to column 15, line 4, which shows counting).

Chrysos further teaches filtering the information based on the thread of execution (see, for example, column 12, lines 1-4), but does not explicitly describe:

wherein the sample filtering and counting logic is replicated on a per thread basis.

Nonetheless, one of ordinary skill in the art could, with predictable results, implement the teachings of Chrysos such that the sample filtering and counting logic is replicated on a per thread basis.

For example, in an analogous art, Kalafatis teaches qualifying events of interest in a multi-threaded processor based on the particular thread that executes the instructions (see, for example, column 2, lines 39-55). Kalafatis describes that such qualification provides versatility in reporting the event information (see, for example, column 6, lines 41-58).

Therefore, in view of Kalafatis, it would have been obvious to those of ordinary skill in the art at the time the invention was made to implement the teachings of Chrysos such that the sample filtering and counting logic is replicated on a per thread basis.

Chrysos in view of Kalafatis further teaches or suggests:

a notification logic, the notification logic reporting to a particular thread the information relating to the instruction if the instruction corresponds to the desired sampled thread (see, for example, column 6, lines 60-65, and see, for example, FIG. 7B and column 17, lines 34-61, which shows reporting the information).

With respect to claim 20 (previously presented), the rejection of claim 18 is incorporated, and Chrysos in view of Kalafatis further teaches or suggests that the sampling register logic includes a register with a bit vector representing events of interest; and

wherein the sampling logic determines whether the instruction includes events of interest by comparing the information relating to the instruction to the bit vector (see, for example, column 16, lines 52-55).

With respect to claim 21 (previously presented), the rejection of claim 18 is incorporated, and Chrysos in view of Kalafatis further teaches or suggests that the information relating to the instruction represents an instruction history (see, for example, column 6, lines 40-45), and the instruction history includes information relating to at least one of an events value, a program counter value, a branch target address value, an effective memory address value, a latency value, a number in issue bundle value, a number in retire bundle value, a privileged value, a branch history value and a number in fetch bundle value (see, for example, column 6, lines 48-49).

With respect to claim 22 (previously presented), the rejection of claim 18 is incorporated, and Chrysos in view of Kalafatis further teaches or suggests that the sampling register logic includes a sample selection criteria register storing sample selection criteria (see, for example, column 16, lines 52-55); and the sample selection criteria include information relating to a desired sampled thread (see, for example, column 15, lines 30-35).

With respect to claim 23 (new), the rejection of claim 1 is incorporated, and Chrysos in view of Kalafatis further teaches or suggests that storing the sampling information further comprises storing the sampling information to a memory register shared by multiple threads (see, for example, column 11, lines 31-38, which shows storing the sampling information to a shared register file in memory).

Conclusion

5. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event,

however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

6. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Michael J. Yigdall whose telephone number is 571-272-3707. The examiner can normally be reached on Monday to Friday from 8:00 AM to 4:30 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tuan Q. Dam can be reached on 571-272-3695. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

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